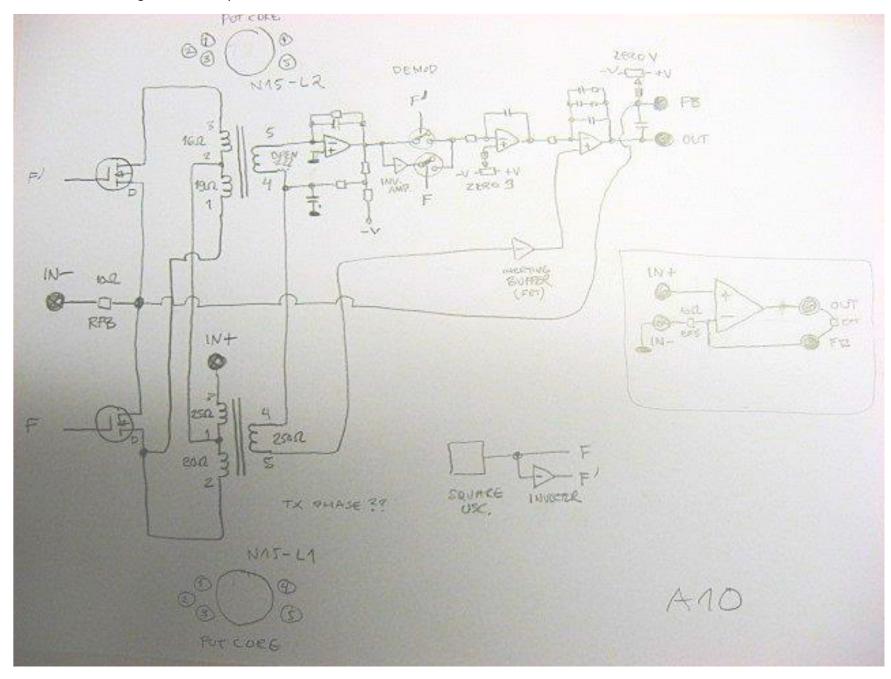
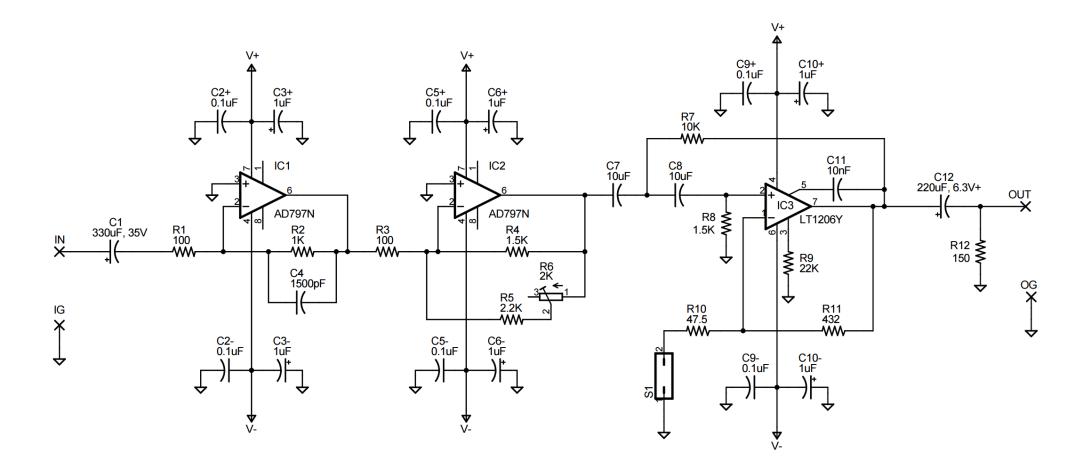
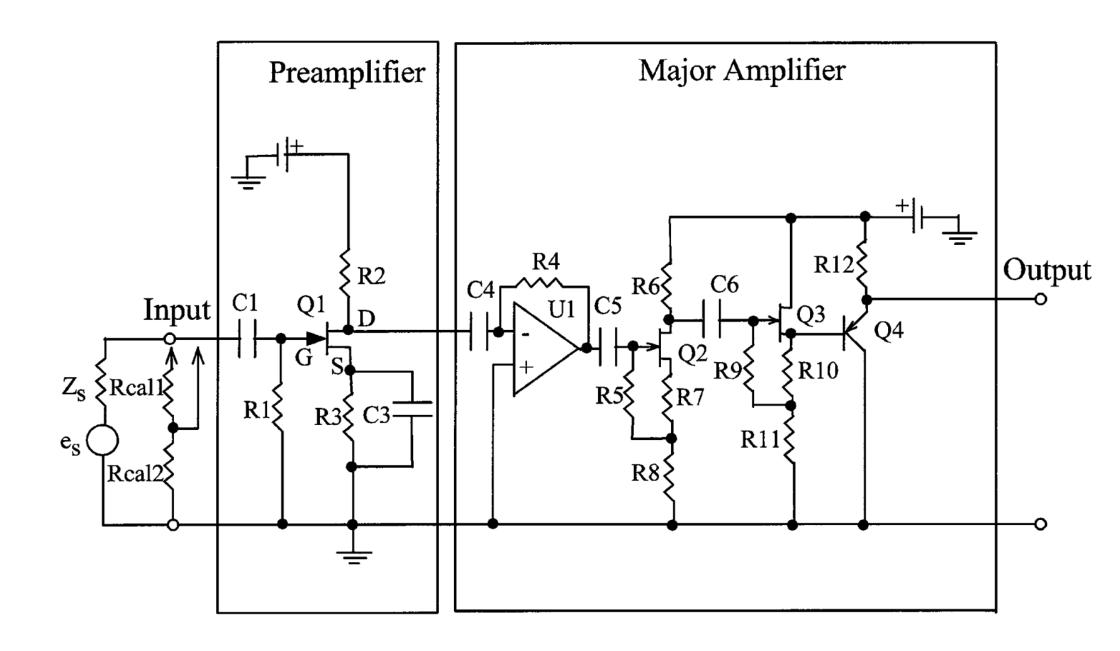
EM Electronics – '90s? – A10 –rough schematic by ltz2000







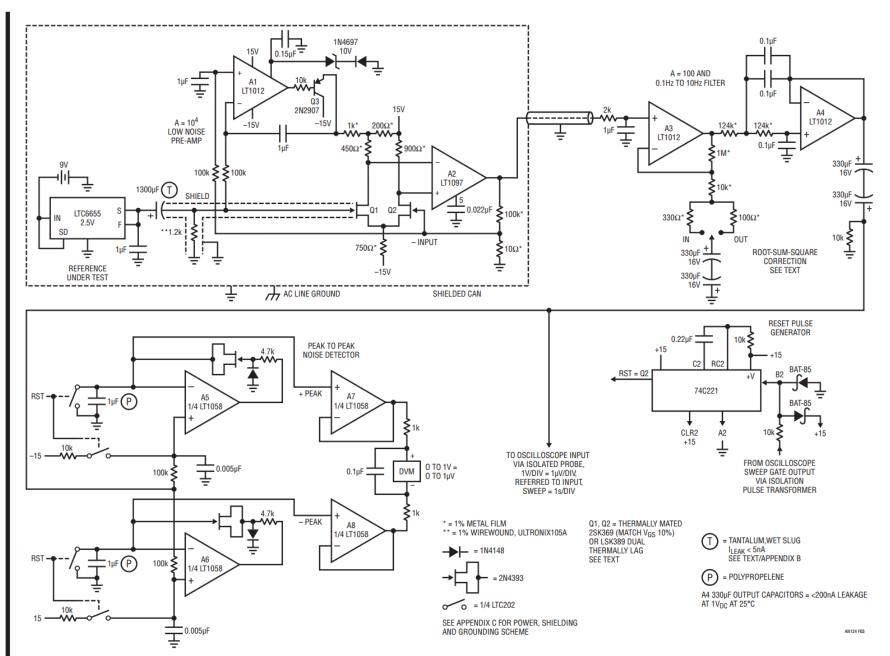


Figure 3. Detailed Noise Test Circuitry. Thermally Lagged Q1-Q2 Low Noise J-FET Pair Is DC Stabilized by A1-Q3; A2 Delivers A = 10,000 Pre-Amplifier Output. A3-A4 form 0.1Hz to 10Hz ,A = 100, Bandpass Filter; Total Gain Referred to Pre-Amplifier Input Is 10^6 . Peak to Peak Noise Detector, Reset by Monitoring Oscilloscope Sweep Gate, Supplies DVM Output

